Effects of Anodic Bonding on Reliability of Sensors and MOS Circuitry

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Anodic bonding is a cost-effective method for wafer-level assembly of MEMS [1]. However, it is important that the anodic bonding process does not deteriorate the electrical properties of the sensor chip. Increased diode leakage current and decreased breakdown voltage of p-n junctions [2] are reported after anodic bonding. With the advent of on-chip integrated CMOS electronics, the chip is potentially more sensitive to processes involving electric fields and elevated temperatures. We are investigating the feasibility of packaging chips including CMOS electronics by anodic bonding technology. We have reported increased oxide charge after bonding [3]. In this experiment, we report that the oxide degradation is smaller when using glass wafers with deep cavities.

In order to investigate the feasibility of packaging chips including CMOS by anodic bonding technology, we used silicon wafers with MOS capacitors with 1000 Å wet grown oxide and aluminium gates. There were two different gate shapes; one solid gate (SG), and one with a finger shape (FG), in order to expose edge effects more clearly. The wafers were bonded to Pyrex #7740 wafers applying -800 V for five minutes at 400°C, in vacuum ambient. There was either 1 µm or 200 µm vertical distance between the Pyrex and the gate metal, as shown in Figure 1. The MOS capacitors were characterised before and after anodic bonding by measuring the flat-band voltage, V_{fb}. We also measured the leakage current I_{gb} between the gate and silicon bulk contact in order to monitor the oxide conductivity. Keithley's WIN-82 system [4] was used for the measurements.

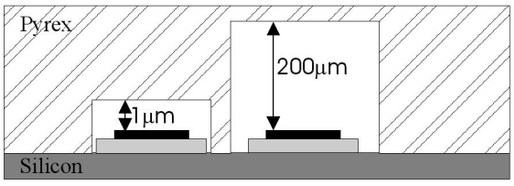
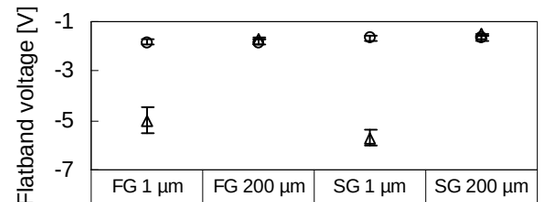


Figure 1: The MOS capacitors have either 1 µm or 200 µm vertical distance to the Pyrex. The MOS oxide is light grey, silicon is dark grey, aluminium is black and Pyrex is drawn as hatched area.

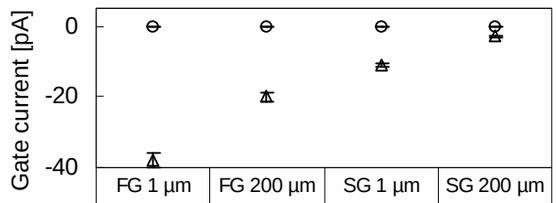
Figure 2 summarises the mean values of V_{fb} before and after anodic bonding for all different MOS parameters. After bonding, the V_{fb} of the capacitors were different depending on the vertical distance to the Pyrex. Capacitors with 1 µm vertical distance to the Pyrex exhibited a negative shift in V_{fb}, indicating increased oxide charge. The shift corresponded to a mean increase in oxide fixed charge of $6.6 \cdot 10^{11} cm^{-2}$ for FG capacitors, and $9.0 \cdot 10^{11} cm^{-2}$ for SG capacitors. All FG and SG capacitors with 200 µm vertical gap had slightly more positive V_{fb} after anodic bonding, probably due to thermal annealing of the oxide [5]. The fact that there was no difference between FG and SG capacitors suggests that the oxide charge increase is independent of gate geometry. The electric field between the Pyrex and the silicon wafer is one such gate geometry-independent component that is likely to affect the gate oxide adversely. An estimation of the electic field indicates that without conducting microplasmas, it would be $2.0 \cdot 10^6$ Vcm^{-1} across the gate oxide of capacitors with 1 µm vertical distance to the Pyrex, and $1.0 \cdot 10^4$ Vcm^{-1} across the gate oxide of capacitors with 200 µm vertical distance to the Pyrex.



	FG 1 µm	FG 200 µm	SG 1 µm	SG 200 µm
○ Before	-1.825	-1.825	-1.667	-1.65
△ After	-5	-1.7	-5.7	-1.5

Figure 2: V_{fb} [V] before (circles) and after (triangles) anodic bonding of the MOS capacitors.

Figure 3 shows the mean values of I_{gb} at 10 V gate bias. The current increased by a factor between 20 and 150 after anodic bonding, indicating increased oxide conductivity, and hence oxide degradation. This degradation was also more severe for capacitors with 1 µm gap than with 200 µm gap, but in addition, FG capacitors were more affected than SG capacitors. The reason for the gate geometry-dependent current increase needs further investigation. The situation with a larger leakage current in the FG capacitors after bonding is expected to occur due to perimeter leakage if the oxide not covered by gate metal is even more damaged than the gate oxide. However, more experiments are necessary to establish if such is the case.



	FG 1 µm	FG 200 µm	SG 1 µm	SG 200 µm
○ Before	-0.225	-0.325	-0.093	-0.117
△ After	-38	-20	-11	-3

Figure 3: I_{gb} [pA] before (circles) and after (triangles) anodic bonding of the MOS capacitors.

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